Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Canceled)

Claim 2 (Currently Amended) A record signal processing circuit comprising:

a coding device for inputting data to be recorded, and coding the input data into a bit stream of a coded word with a parity; ~~and~~

a bit converting circuit for inputting an output of said coding device and bit converting a coded bit stream of a coded word with a parity; and

a precoder for inputting an output of said ~~coding device~~bit converting circuit, and performing precoding according to 1/(1+D) as a delay operator,

wherein said coding device calculates a parity bit with a pattern corresponding to an output of said precoder before the precoding, ~~and~~

wherein said bit converting circuit performs bit conversion with a bit stream containing the parity bit, and

wherein said precoder outputs data to be recorded as a bit stream of a coded word with a coded parity.

Claim 3 (Currently Amended) ~~The~~A record signal processing circuit ~~according to claim 2,~~comprising:

a coding device for inputting data to be recorded, and coding the input data into a bit stream of a coded word with a parity;

a bit converting circuit for inputting an output of said coding device and bit converting a coded bit stream of a coded word with a parity; and

a precoder for inputting an output of said bit converting circuit, and performing precoding according to 1/(1+D) as a delay operator,

wherein said coding device calculates a parity bit with a pattern corresponding to an output of said precoder before the precoding,

wherein said bit converting circuit performs bit conversion with a bit stream containing the parity bit,

wherein said precoder outputs data to be recorded as a bit stream of a coded word with a coded parity, and

wherein, when performing the bit conversion with the bit stream containing the parity bit, said coding device performs either conversion of bit patterns "*01-1-110", "011-1-10*" and "011-1-110" (* is don't care) with the parity bit being "0", or conversion of a bit pattern "011-1-110" with the parity being "0", where a bit stream of a coded word of 3 bits immediately before the parity bit, one bit of the parity bit, and a bit stream of a coded word of 3 bits immediately after the parity bit are separated by a symbol "-".

Claim 4 (Currently Amended) An information recording apparatus including a record signal processing circuit according to claim 3, comprising:

~~a record signal processing circuit according to claim 3;~~

an information recording medium for recording data; and

a recording head for recording data on said information recording medium, wherein:

said information recording apparatus inputs data to be recorded,

said record signal processing circuit converts input data into a bit stream of a coded word with a parity, and

said recording head records the data on said information recording medium according to the bit stream of the coded word with the parity.

Claim 5 (Original) The information recording apparatus according to claim 4, wherein the data recorded on said information recording medium has a continuous number "r" not larger than 3 or 4 of reverse times of record state of recorded information.

Claim 6 (Currently Amended) An information recording apparatus comprising:

a coding device for inputting data to be recorded, and coding the input data into a bit stream of a coded word;

a parity generating circuit for inputting the bit stream of the coded word from said coding device, generating a parity bit for error detection, and adding the parity bit to the bit stream of the coded word;

a bit converting circuit for inputting an output of said parity generating circuit and bit converting a bit stream of a coded word to which the parity bit is added;

a precoder for inputting an output of said ~~parity generating circuit,~~bit converting circuit and performing precoding according to 1/(1+D) as a delay operator;

an information recording medium for recording data; and

a recording head for recording data on said information recording medium,

wherein said recording head records data on said information recording head according to the bit stream of the coded word outputted from said precoder, and

wherein said recording is performed in such a manner that a value of a parity bit resulting from parity calculation of a bit stream as a target of the parity bit among bit streams recorded on said information recording medium does not necessarily coincide with a value of a parity bit recorded on said information recording medium correspondingly to the bit stream recorded on said information recording medium.

Claim 7 (Currently Amended) ~~The~~An information recording apparatus ~~according to claim 6,~~comprising:

a coding device for inputting data to be recorded, and coding the input data into a bit stream of a coded word;

a parity generating circuit for inputting the bit stream of the coded word from said coding device, generating a parity bit for error detection, and adding the parity bit to the bit stream of the coded word;

a bit converting circuit for inputting an output of said parity generating circuit and bit converting a bit stream of a coded word to which the parity bit is added;

a precoder for inputting an output of said bit converting circuit and performing precoding according to 1/(1+D) as a delay operator;

an information recording medium for recording data; and

a recording head for recording data on said information recording medium,

wherein said recording head records data on said information recording head according to the bit stream of the coded word outputted from said precoder,

wherein said recording is performed in such a manner that a value of a parity bit resulting from parity calculation of a bit stream as a target of the parity bit among bit streams recorded on said information recording medium does not necessarily coincide with a value of a parity bit recorded on said information recording medium correspondingly to the bit stream recorded on said information recording medium, and

wherein said recording is performed in such a manner that a value of the parity bit is always "0", where a value of a parity bit resulting from parity calculation of a bit stream as a target of the parity bit among bit streams recorded on said information recording medium does not coincide with a value of a parity bit recorded on said information recording medium correspondingly to the bit stream recorded on said information recording medium.

Claim 8 (Currently Amended) ~~The~~An information recording apparatus ~~according to claim 7,~~comprising:

a coding device for inputting data to be recorded, and coding the input data into a bit stream of a coded word;

a parity generating circuit for inputting the bit stream of the coded word from said coding device, generating a parity bit for error detection, and adding the parity bit to the bit stream of the coded word;

a bit converting circuit for inputting an output of said parity generating circuit and bit converting a bit stream of a coded word to which the parity bit is added;

a precoder for inputting an output of said bit converting circuit and performing precoding according to 1/(1+D) as a delay operator;

an information recording medium for recording data; and

a recording head for recording data on said information recording medium,

wherein said recording head records data on said information recording head according to the bit stream of the coded word outputted from said precoder,

wherein said recording is performed in such a manner that a value of a parity bit resulting from parity calculation of a bit stream as a target of the parity bit among bit streams recorded on said information recording medium does not necessarily coincide with a value of a parity bit recorded on said information recording medium correspondingly to the bit stream recorded on said information recording medium,

wherein said recording is performed in such a manner that a value of the parity bit is always "0", where a value of a parity bit resulting from parity calculation of a bit stream as a target of the parity bit among bit streams recorded on said information recording medium does not coincide with a value of a parity bit recorded on said information recording medium correspondingly to the bit stream recorded on said information recording medium, and

wherein data recorded on said information recording medium has a continuous number "r" not larger than 3 or 4 of reverse times of record state of recorded information.

Claim 9 (Original) A reproduction signal processing circuit for reproducing data, comprising:

a filter;

an analog-to-digital converter;

an equalizing circuit;

a Viterbi decoding circuit; and

a decoder,

wherein:

said filter inputs a reproduction signal reproduced from a medium which records information, and rejects high frequency noises therefrom;

said analog-to-digital converter converts the signal whose high frequency noises have been rejected into a digital signal;

said equalizing circuit equalizes the digital signal into an equalized signal;

said Viterbi decoding circuit performs data discrimination, and outputs a discriminated bit stream;

said decoder decodes the discriminated bit stream into data, the discriminated bit stream having a 1's continuous number "r" not larger than 3 or 4, and one parity bit being provided at least one place between coded words;

said Viterbi decoding circuit performs data discrimination by excluding from search candidates a transition path corresponding to a coded word series "1111" in a process of searching a most likelihood path corresponding to a case where the 1's continuous number "r" is 3, or by excluding from search candidates a transition path corresponding to a coded word series "11111" in a process of searching a most likelihood path corresponding to a case where the 1's continuous number "r" is 4, or

by excluding from search candidates transition paths corresponding to coded word series "11111", "001111" and "111100", in a process of searching a most likelihood path corresponding to a case where the 1's continuous number "r" is 4; and

said decoder includes a bit reverse-converting circuit and an error correction circuit, in which said bit reverse-converting circuit performs reverse-conversion of discriminated bit stream in a case of a bit stream of either "****-0-1110" or "0111-0-****" (* is don't care), where a bit stream of a coded word of 4 bits immediately before the parity bit, one bit of the parity bit, and a bit stream of a coded word of 4 bits immediately after the parity bit are separated by a symbol "-", and said error correction circuit corrects discrimination errors of 1 bit and 3 bits.

Claim 10 (Currently Amended) An information reproducing apparatus including a reproduction signal processing circuit according to claim 9, comprising:

an information recording medium for recording data; and

a reproducing head for reproducing data recorded on said information recording medium; ~~and~~

~~a reproduction signal processing circuit according to claim 9,~~

wherein said reproducing head obtains a reproduction signal from said information recording medium, and

wherein said ~~information reproducing~~reproduction signal processing circuit inputs the reproduction signal, and outputs reproduced data.

Claim 11 (Original) The information reproducing apparatus according to claim 10, wherein the data recorded on said information recording medium has a

continuous number "r" not larger than 3 or 4 of reverse times of record state or recorded information.

Claim 12 (Currently Amended) An information recording and reproducing circuit comprising:

a record signal processing circuit including:

a coding device for inputting data to be recorded, and coding the input data into a bit stream of a coded word with a parity; and

a precoder for inputting an output of said coding device, and performing precoding according to 1/(1+D) as a delay operator,

wherein said coding device calculates a parity bit with a pattern corresponding to an output of said precoder before the precoding, and performs bit conversion with a bit stream containing the parity bit,

wherein said precoder outputs the data to be recorded as a bit stream of a coded word with a coded parity, and

wherein, when performing the bit conversion with the bit stream containing the parity bit, said coding device performs either conversion of bit patterns "*01-1-110", "011-1-10*" and "~~001-1-110~~011-1-110" (* is don't care) with the parity bit being "0", or conversion of a bit pattern "011-1-110" with the parity being "0", where a bit stream of a coded word of 3 bits immediately before the parity bit, one bit of the parity bit, and a bit stream of a coded word of 3 bits immediately after the parity bit are separated by a symbol "-"; and

a reproduction signal processing circuit for reproducing data, including:

a filter;

an analog-to-digital converter;

an equalizing circuit;

a Viterbi decoding circuit; and

a decoder,

wherein:

said filter inputs reproduction signal reproduced from a medium recording information, and rejects high frequency noises,

said analog-to-digital converter converts the signal whose frequency noises have been rejected into a digital signal;

said equalizing circuit equalizes the digital signal into an equalized signal;

said Viterbi decoding circuit performs data discrimination, and outputs a discriminated bit stream;

said decoder decodes the discriminated bit stream into data, the discriminated bit stream having a 1's continuous number "r" not larger than 3 or 4, and one parity bit being provided at least one place between coded words;

said Viterbi decoding circuit performs data discrimination by excluding from search candidates a transition path corresponding to a coded word series "1111" in a process of searching a most likelihood path corresponding to a case where the 1's continuous number "r" is 3, or by excluding from search candidates a transition path corresponding to a coded word series "11111" in a process of searching a most likelihood path corresponding to a case where the 1's continuous number "r" is 4, or by excluding from search candidates transition paths corresponding to coded word series "11111", "001111" and "111100", in a process of searching a most likelihood path corresponding to a case where the 1's continuous number "r" is 4; and

said decoder includes a bit reverse-converting circuit and an error correction circuit, in which said bit reverse-converting circuit performs reverse-conversion of discriminated bit stream in a case of a bit stream of either "****-0-1110" or "0111-0-****" (* is don't care), where a bit stream of a coded word of 4 bits immediately before the parity bit, one bit of the parity bit, and a bit stream of a coded word of 4 bits immediately after the parity bit are separated by a symbol "-", and said error correction circuit corrects discrimination errors of 1 bit and 3 bits.

Claim 13 (Currently Amended) An information recording and reproducing apparatus including an information recording and reproducing circuit according to claim 12, comprising:

an information recording medium for recording data; and

a recording/reproducing head for recording/reproducing data on/from said information recording medium~~; and~~

~~an information recording and reproducing circuit according to claim 11,~~

wherein the data recorded on said information recording medium has a continuous number "r" not larger than 3 or 4 of reverse times of record state of recorded information.

Claim 14 (Currently Amended) An information recording an reproducing apparatus including a reproduction signal processing circuit according to claim 9, comprising:

an information recording apparatus including:

a coding device for inputting data to be recorded, and coding the input data into a bit stream of a coded word with a parity; and

a precoder for inputting an output of said coding device, and performing precoding according to 1/(1+D) as a delay operator,

wherein said coding device calculates a parity bit with a pattern corresponding to an output of said precoder before the precoding, and performs bit conversion with a bit stream containing the parity bit;

wherein said precoder outputs the data to be recorded as a bit stream of a coded word with a coded parity; and

wherein, when performing the bit conversion with the bit stream containing the parity bit, said coding device performs either conversion of bit patterns "*01-1-110", "011-1-10*" and "011-1-110" (* is don't care) with the parity bit being "0", or conversion of a bit pattern "011-1-110" with the parity being "0", where a bit stream of a coded word of 3 bits immediately before the parity bit, one bit of the parity bit, and a bit stream of a coded word of 3 bits immediately after the parity bit are separated by a symbol "-",

said information recording apparatus further includes:

an information recording/reproducing medium for recording and reproducing data; and

a recording/reproducing head for recording/reproducing data on/from said information recording/reproducing medium,

wherein said information recording apparatus inputs data to be recorded;

wherein said information recording apparatus converts input data into a bit stream of a coded word with a parity; and

wherein said recording/reproducing head records the data on said information recording/reproducing medium according to the bit stream of the coded word with the parity;~~,~~

~~an information reproducing apparatus including a reproduction signal processing circuit according to claim 8,~~

wherein said recording/reproducing head obtains a reproduction signal from said information recording medium, and said information reproducing apparatus inputs the reproduction signal and outputs reproduced data; and

wherein the data recorded on said information recording medium has a continuous number "r" not larger than 3 or 4 of reverse times of record state of recorded information.

Claim 15 (Currently Amended) A magnetic disk apparatus <u>including an information recording and reproducing circuit according to claim 12,</u> comprising:

a magnetic disk as an information recording medium for recording/reproducing data by using magnetic changes;

a magnetic recording/reproducing head for recording/reproducing data on/from said magnetic disk;

an interface circuit connected to an external device; <u>and</u>

a hard disk controller for transmitting/receiving data to/from said interface circuit~~; and~~,

~~an~~<u>wherein said</u> information recording and reproducing circuit ~~according to claim 12 for performing~~<u>performs</u> signal processing of data outputted from said hard disk controller.

Claim 16 (Original) The magnetic disk apparatus according to claim 15, wherein the data recorded on said magnetic disk has a continuous number "r" not larger than 3 or 4 of reverse times of magnetization which is record state of recorded information on a bit basis.